REMARKS

In this Response, none of the claims are amended or cancelled, and no new claims are added. Claims 1-7 are presented for examination.

Examiner Interview

The applicants thank the Examiner for the courtesies extended during an interview on October 16, 2008 (hereinafter "Interview"). In the Interview, features of claim 1 were discussed in view of the cited references. However, no conclusion on patentability was reached.

Rejections Under 35 U.S.C. § 103

Claims 1- 4 and 6-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curry et al. (US 6,112,275) in combination with Smith et al. (US 6,762,733). The applicants respectfully traverse the rejection for at least the following reasons.

Claim 1 is directed towards a programmable interface that includes, among other features a system processor that is *configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.*

For example, the applicants' Fig. 1 illustrates a main system CPU 30 loading executable code onto the Code Store SRAM 14, and signaling the microcontroller 12, via the run control register 16, to begin execution of one or more instructions included in the executable code.[1]

The Examiner alleged that Curry discloses a programmable interface, but acknowledged that Curry does not disclose at least the above recited features (page 12 of the office action). The Examiner, however, alleged that Smith discloses the same.

Specifically, the Examiner alleged that Smith discloses, in Fig. 7, registers 160, 162 and 164, which the Examiner appears to equate with the recited *run control register.* Smith discloses that the registers 160, 162 and 164 are coupled to the PSRAM controller 166. The bits stored in the respective registers are input to the PSRAM controller 166 which, in turn, selects, in accordance with the state of the output from registers 158-164, the address mapping mode of

[1] Applicants specification, paragraph 14, lines 1-5.

PSRAM 174.[2] The Examiner appears to equate Smith's PSRAM controller 166's selecting the PSRAM 174 address mapping mode with the recited *execution of instructions included in an executable code*.

Claim 1 recites four components: a *system processor,* a *Code Store SRAM,* a *microcontroller,* and a *run control register.* Additionally, claim 1 recites that the *system processor* loads executable codes onto the *Code Store SRAM.* Furthermore, claim 1 recites that *the system processor signals the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.*

Fig. 7 of Smith illustrates registers 160-164 coupled to the PSRAM controller 166, and further illustrates the PSRAM controller 166 coupled to the PSRAM 174. The Examiner equated registers 160-164 with the recited *run control register*. The Examiner, however, has not clearly identified any component in Smith that is equivalent to the recited *Code Store SRAM.* If, *arguendo*, Smith's PSRAM 174 is equated with the *Code Store SRAM*, then a system processor in Smith needs to load executable code onto the PSRAM 174, as recited in claim 1. Smith, however, does not disclose a *system processor* loading any executable code onto the PSRAM 174. Also if, *arguendo*, Smith's PSRAM controller 166 is equated with the recited *system processor*, then Smith lacks a *microcontroller*, as recited in claim 1. On the other hand, if Smith's PSRAM controller 166 is equated with the recited *microcontroller*, then the PSRAM controller 166 needs to execute codes stored in the PSRAM 174; however, it is respectfully submitted that Smith does not disclose any such feature.

Further, Smith discloses that applications programs may be downloaded from the host computer, buffered in the FIFO 184, and loaded into the pseudo-static RAM 174 via the SNES data bus.[3] Smith also discloses that programs stored in PSRAM 174 (allegedly equated with the recited *Code Store SRAM*) may be accessed by the host CPU 220 via address busses and data buses (see FIG. 9).[4] If, *arguendo*, Smith's host CPU 220 is equated with the recited *microcontroller,* Smith fails to disclose a *system processor* that loads the programs onto the

---

[2] Smith, col. 13, lines 3-7.
[3] Smith, col. 16, lines 26-28.
[4] Smith, col. 17, lines 60-63.

PSRAM 174 and also instructs the host CPU 220, via a *run control register,* to execute the programs stored in the PSRAM 174.

For at least these reasons, the applicants respectfully submit that Smith fails to disclose or suggest the above recited features. The Examiner also acknowledged in the Office Action mailed August 19, 2008 that Curry does not cure these deficiencies of Smith. Accordingly, the applicants respectfully submit that neither Curry, nor Smith, either alone or in combination, disclose or even suggest the features of claim 1, and accordingly, respectfully submit that claim 1 is in condition for allowance, along with associated dependent claims 2-4 and 6-7.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Curry in combination with Smith and further in view of Ueda (US 5,631,637).

Claim 5 depends from allowable claim 1. It is respectfully submitted that Ueda does not cure the deficiencies of Curry and Smith, as applied to claim 1. Accordingly, the applicants respectfully submit that claim 5 is allowable for at least the reasons claim 1 is allowable.

Conclusion

For at least these reasons, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (503) 796-2084. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge Deposit Account No. 500393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 10/20/2008

/Kevin T. LeMond/
Kevin T. LeMond
Reg. No. 35,933

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981